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10/524,203	02/10/2005	Hiroaki Ozeki	MAT-8657US	9927

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RATNERPRESTIA
P O BOX 980
VALLEY FORGE, PA 19482-0980

EXAMINER	
TIMORY, KABIR A	
ART UNIT	**PAPER NUMBER**
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/524,203	OZEKI ET AL.	
	Examiner	Art Unit	
	KABIR A. TIMORY	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 13 June 2008.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-10 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination (RCE) Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 06/13/2008 has been entered.

Response to the Arguments

2. This office action is in response to the amendment filed on 06/13/2008. Claims 1-10 are pending in this application and have been considered below.

3. Applicant arguments regarding the rejection under 35 USC 102(e) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (figure 5, specification, page 1, lines 10-27, and page 2, lines 1-2) in view of Hayashi et al. (US 6,075,829) have been fully considered but they are not persuasive. The examiner thoroughly reviewed Applicant's arguments but firmly believes that the cited reference reasonably and properly meets the claimed limitation as rejected.

Applicant's argument: "Fig. 1 of Hayashi shows frequency divider 35 and multiplier 11. Hayashi's multiplier 11, however, is a heterodyning multiplier (not a frequency multiplier). For example, heterodyning multiplier 11 (as taught by Hayashi) multiples a sinusoid output from oscillator 31 (for example cos(F1}) with another sinusoid from port 10 (for example cos(F2)). These two sinusoids are multiplied together in a heterodyning procedure wherein the output of the multiplier produces two new sinusoids with different frequencies. One of the new sinusoid frequencies produced by heterodyning multiplier 11 is at the sum of the two input frequencies (F1 + F2) and the other is at the difference of the two input frequencies (F1 - F2) (not the product of the two frequencies F1 * F2):

*cos (1:1) * cos (F2) = .5 * ((cos (F1 + F2) +cos (F1 - F2))*

Applicants' claim 1 is different then Hayashi because the addition of a **frequency** multiplier which produces a frequency which is the **product** of the frequency divider output and a magnitude of the frequency multiplier. <u>For example, in Applicants' Fig. 1, frequency multiplier 5 multiples the frequency of the sinusoid output of frequency divider 4. If the sinusoid output of frequency divider 4 has a frequency *cos(Fin)*, and frequency multiplier 5 has a magnitude N, then the frequency of the output sinusoid *cos(Four)* of the frequency multiplier 5 would be the product of the two:</u>

<u>Frequency of divider output *cos(**Fin**)*</u>

<u>Magnitude of frequency multiplier N</u>

<u>Product of frequency multiplier *cos(**Fout**)* = *cos(**Fin** * **N**)*</u>

Thus, Hayashi's multiplier is a heterodyning multiplier which produces sinusoids with frequencies at the sum ***cos*** (1 + F2) and difference cos *(FI - F2)* of the input frequencies, whereas Applicants' frequency multiplier produces a sinusoid with a frequency that is the product between the input sinusoid frequency and the multiplier magnitude *cos(Fin * N).* Therefore, combining Hayashi and AAPA would not teach the features of Applicants' claim 1 (Hayashi's multiplier is not a frequency multiplier).

Examiner's response: First of all, the examiner would like to point out that mathematical analysis of the applicant is incorrect because of a simple mathematical reason as below:

For example:

If the frequency of the divider output is: ***cos(Fin)***

And if the magnitude of the multiplier is ***N***

Then the product of the output of the divider and frequency multiplier is:

cos(Fin) X N = <u>N cos(Fin)</u>

Not

<u>cos(Fin * N)</u>.

There's a big difference between these two results.

The applicant's calculation as suggest in the above argument would <u>change the phase (angle) of the signal not the magnitude</u>. Therefore the correct output of the multiplier is ***<u>N cos(Fin)</u>***, where N is the magnitude of the signal.

Accordingly, the examiner is respectfully requesting the applicant to clarify the arguments above.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-10 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In claim 1, line 9, the claim recite a limitation "**a magnitude of the frequency multiplier**". This limitation is not described in the specification and the examiner is unable to find any support for this limitation in the specification. Therefore, the claim is failing to comply with the enablement requirement.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

(1) Claim 1 recites the limitation "**the frequency**" in line 5. There is insufficient antecedent basis for this limitation in the claim.

(2) Claim 1 recites the limitation "**the frequency multiplier**" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (figure 5, specification, page 1, lines 10-27, and page 2, lines 1-2) in view of Hayashi et al. (US 6,075,829).

Regarding claim 1:

As shown in figure 5, AAPA a digital signal receiver comprising:

- a reference signal generator (101 in figure 5) for generating a first reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2);
- a base band transform circuit (108 in figure 5) for converting a first high-frequency signal with digital modulation into a base band signal with using the first reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2); and

- a digital demodulator (110 in figure 5) to demodulate a signal output from the base band transform circuit with using the signal output from the frequency multiplier as a reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2);
- wherein the first reference signal is generated independent of the signal output of the frequency multiplier (signal generator of figure 5 (AAPA) illustrates the same configuration as figure 1 and 3 of the instant application. Therefore, the examiner is interpreting that the first reference signal is generated independent of the signal output of the frequency multiplier) (101 in figure 5).

AAPA et al. discloses all of the subject matter as described above except for specifically teaching a frequency divider to divide the frequency of the first reference signal; a frequency multiplier divider wherein an output frequency of the frequency multiplier is a product of the divided first reference signal produced by the frequency divider and a magnitude of the frequency multiplier.

However, Hayashi et al. in the same field of endeavor, teaches a frequency divider (35 in figure 1) to divide the frequency of the first reference signal; a frequency multiplier divider wherein an output frequency of the frequency multiplier is a product of the divided first reference signal produced by the frequency divider and a magnitude of the frequency multiplier (in figure 1, Hayashi et al. clearly disclose that the output of the frequency divider 33 is sent to the filter 37 via phase detector 34 and then sent to the multiplier 11 via oscillator 31. Thus the multiplier multiplies the output of the divider by some value) (see figure 1).

One of ordinary skill in the art would have clearly recognized that phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. In digital communication system, frequency dividers are used along with filters and multipliers to produce signals such that any difference between the inputs to the multiplier results in a proportional signal being output from the filter until a steady state output is produced. Also, using frequency divider, a filter and a multiplier reduce the noise level in the system. In order reduce the noise level due to the high power, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider, a filter and a multiplier as taught by Hayashi et al. in method and system of (AAPA) to reduce noise level in the system. By doing so, we can reduce the amount of noise level in the system and also we can produce an output signal proportional to the reference signal.

Regarding claim 2:

AAPA et al. further discloses a frequency converter (102 in figure 5) for receiving a second high-frequency signal modulated by the digital signal and converting a frequency of the second high-frequency signal to generate the first high-frequency signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 3:

AAPA et al. further discloses wherein the frequency converter converts the second high-frequency signal into the first high-frequency signal with using the first reference signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 4:

AAPA et al. further discloses wherein the first high-frequency signal is modulated by the digital signal by Orthogonal Frequency Division Multiplexing system (110 in figure 5), and the digital demodulator comprises an Orthogonal Frequency Division Multiplexing demodulator (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 5:

AAPA et al. further discloses wherein the base band transform circuit comprises an orthogonal base band transform circuit (108 in figure 5) operable to convert the first high-frequency signal into a first base band signal and a second base band signal orthogonal each other and output the first base band signal and the second base band signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 6:

AAPA et al. further discloses wherein the orthogonal base band transform circuit includes a 90°-phase shifter for shifting a phase of the first reference signal by 90 degrees (base-band orthogonal transform circuit is interpreted to generate signal which are shifted 90 degree from each other such as I and Q signal) (108 in figure 5), a first mixer (102 in figure 5) for mixing the first reference signal with the first high-frequency signal to convert the first high-frequency signal into the first base band signal, and a second mixer (108 in figure 5) for mixing the second reference signal with the first high-frequency signal to convert the first high-frequency signal into the second base band signal (specification, page 1, lines 10-27, and page 2, lines 1-2).

Regarding claim 7:

AAPA et al. discloses all of the subject matter as described above except for specifically teaching a device including the frequency divider and at least one of the base band transform circuit and the frequency converter.

However, Hayashi et al. in the same field of endeavor, teaches a device including the frequency divider and at least one of the base band transform circuit and the frequency converter (35 in figure 1).

One of ordinary skill in the art would have clearly recognized that phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. In digital communication system, frequency dividers are used along with filters and multipliers to produce signals such that any difference between the inputs to the multiplier results in a proportional signal being output from the filter until a steady state output is produced. Also, using frequency divider, a filter and a multiplier reduce the noise level in the system. In order reduce the noise level due to the high power, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider, a filter and a multiplier as taught by Hayashi et al. in method and system of (AAPA) to reduce noise level in the system. By doing so, we can reduce the amount of noise level in the system and also we can produce an output signal proportional to the reference signal.

Regarding claim 8:

AAPA et al. further discloses a device including the digital demodulator (110 in figure 5) and the frequency multiplier (109 in figure 5).

Regarding claim 9:

AAPA et al. discloses all of the subject matter as described above except for specifically teaching a low-pass filter for receiving a signal output from the frequency divider and outputting a signal to the frequency multiplier.

However, Hayashi et al. in the same field of endeavor, teaches a low-pass filter (37 in figure 1) for receiving a signal output from the frequency divider (35 in figure 1) and outputting a signal to the frequency multiplier (11 in figure 1).

One of ordinary skill in the art would have clearly recognized that phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. In digital communication system, frequency dividers are used along with filters and multipliers to produce signals such that any difference between the inputs to the multiplier results in a proportional signal being output from the filter until a steady state output is produced. Also, using frequency divider, a filter and a multiplier reduce the noise level in the system. In order reduce the noise level due to the high power, it would have been obvious to one ordinary skill in the art at the time the invention was made to use frequency divider, a filter and a multiplier as taught by Hayashi et al. in method and system of (AAPA) to reduce noise level in the system. By doing so, we can reduce the amount of noise level in the system and also we can produce an output signal proportional to the reference signal.

Regarding claim 10:

(AAPA) further discloses a further device including the digital demodulator (110 in figure 5) and the frequency multiplier (109 in figure 5).

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KABIR A. TIMORY whose telephone number is (571)270-1674. The examiner can normally be reached on 6:30 AM - 3:00 PM Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kabir A Timory/
Examiner, Art Unit 2611
/Shuwang Liu/
Supervisory Patent Examiner, Art Unit 2611